characterized as inherently disclosing an output node. Any inherency arguments, however, must satisfy certain requirements repeatedly enunciated by the U.S. Courts of Appeals for the Federal Circuit. Here, these requirements are not met.

"The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." M.P.E.P. § 2112(IV) (quoting *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art)). "To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Id.* (quoting *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)).

In the Office Action, a basis or technical reasoning for having the claimed output node in Wu is *not* provided. For example, there is no rationale for having an output node between the NMOS transistors M1 and M3 to reasonably support the determination that the output node of claim 1 is necessarily present. To the contrary, Wu merely discloses having a connection between the NMOS transistor M1 and M3 and a V_{out} at an *entirely different location* at the transistor Q_3. Because "inherency, however, may not be established by probabilities or possibilities," and "[t]he mere fact that a certain thing may result from a given set of circumstances is not sufficient," Wu cannot inherently disclose an output node and thus, claim 1 is not anticipated by Wu. *Id.* Similarly, claim 3 is not anticipated by Wu.

In addition, Applicant submits that Wu fails to disclose or suggest, inter alia, a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to *an output*

node from a power source voltage as applied. Although the Examiner states that the node between NMOS transistors M1 and M3 corresponds to the claimed output node, this "output node" is connected to the drain of PMOS transistor M1, to the drain and the gate of the NMOS transistor M3, and the gates of the NMOS transistors M4, M5, and M6. Therefore, Wu cannot possibly disclose an output node as recited in claim 1.

Similarly, Wu fails to disclose or suggest an output node wherein a second capacitor is connected between the second common node and the output node, as recited in claim 3. The Examiner characterizes a node between M4 and M6 as corresponding to the claimed output node. This node, however, is merely connected to the capacitor C1, the gates of M3 and M4, the source/drain of M4, and the source/drain of M6, and not to any output. For at least the above reasons, claim 3 is believed to be patentable.

Rejections of Claims 1-4 under § 103(a) over Yamazaki in view of Wu

Claim 1 is believed to be patentable because Yamazaki in view of Wu fail to teach, suggest or provide motivation for, *inter alia*, the claimed output node as recited in the claim. There is nothing in the references which supports the conclusion that the claimed output node is necessarily present in the combination of Yamazaki and Wu. Therefore, Yamazaki in view of Wu cannot inherently disclose such an output node. Therefore, claims 1 and 3 are believed to be patentable.

In addition, Yamazaki and Wu do not expressly disclose the claimed output node. Although the Examiner mentions nodes N11 or N12 of Yamazaki, there is nothing in Yamazaki that suggests that these nodes correspond to the claimed output node. Instead, the node N11 is connected to the drain and the gate of the PMOS 104, the gate of the PMOS 106, the gate of the

PMOS transistor 116, the drain of the NMOS transistor 118, and the drain of the NMOS transistor 112. Node N12 is connected to the drain of the PMOS transistor 105, the drain of the PMOS transistor 120, and the gate and the drain of the NMOS transistor 110. Therefore, claim 1 is believed to be patentable.

Claim 3 is believed to be patentable because the node between the PMOS transistor 126 and the NMOS transistor 128 are not connected to any sort of an output node. Thus, claim 3 is believed to be patentable.

Claim 2, which depends from claim 1, and claim 4, which depends from claim 3 are patentable for at least the reasons submitted for their respective base claims.

In addition, claim 4 is patentable because Yamazaki in view of Wu fail to teach, suggest or provide motivation for all elements of the claim. Claim 4 recites, *inter alia*:

> 4. (original): The bias circuit as claimed in claim 3, wherein the bias circuit part includes:
>
> . . . ;
>
> a fourth PMOS transistor having *a gate and a drain thereof connected to a gate of the first PMOS transistor to form a second common node*, and having a source thereof connected to the drain of the second PMOS transistor;
>
> a first NMOS transistor having a *drain and a gate thereof connected to a drain of the third PMOS transistor to form the output node*, and having a source thereof connected to a grounded power source;
>
> . . . .

In the Office Action, the Examiner argues that PMOS 106 and PMOS 124 of Fig. 5 in Yamazaki correspond to the claimed first PMOS and the fourth PMOS. Assuming *arguendo*, that the Examiner is correct, the PMOS 124 does *not* have a gate and a drain thereof connected to a gate of the PMOS 106. Rather, the gate and the drain of the PMOS 124 are connected to the

gate of the PMOS 126 which the Examiner characterizes as corresponding to the claimed third PMOS transistor.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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